Quark™ Electrical Interface Description Document (IDD)

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1 Document

1.1 Revision History

Version	Date	Comments
100	11/07/2011	Initial Release
101	10/22/2013	• Corrected an error in the caption of Figure 1 • Corrected Table 2 to have EXT_SYNC as input or output • 3.1.1 Added recommendation for connector strain relief • 3.1.6.2 Noted that FLIR does not recommend slave mode for analog video
110	06/09/2014	Modified to reflect Quark 2.0 interface. Specifically, the following has changed and is highlighted in blue text throughout the document: • 3.1.2 Added Quark 2.0 power dissipation (Table 5) and Note2 • 3.1.4.1 Removed BT.656 note about only digital output with color/symbols • 3.1.4.2 Updated CMOS digital output options, clock rate for 640, 60Hz option, FFC notes • 3.1.4.3 Updated LVDS digital output options, clock rate for 640, 60Hz option, line timing details, and FFC notes. Updated Figure 5 for line timing specifics. • 3.1.6.1/3.1.6.2 Updated External Sync behavior • Updated Figure 3 to include (b) and (c) images for YCbCr modes • Updated Table 1 to redefine pin 56 from "reserved" to "XP1_CLK2". Changed pin 55 from "XP1_CLKOUT" to "XP1_CLK1". • Updated Table 2 to include new 16-bit CMOS pin assignments. Note that this mode utilizes pin 56, which was currently unused in any of the XP1 modes. Therefore, pin 56 is added to the table. • Updated Table 6: Included 640, 60Hz option and Digital eZoom mode effect on frame rate and resolution (notes 4 and 5) • Updated Table 7: Included 640, 60Hz option Other changes include: • 3.1.1 Clarified connector height and P/N. • 3.1.1 Corrected Shutter0 and Shutter1 naming convention (labels were swapped wrt Product Spec operation) • 3.1.2 Added note about power interruption during flash operations. • 3.1.7 Clarified voltage: OK to apply more than 3.3 V to serial input.

1.2 Scope

Quark ™ is a miniature infrared imaging core from FLIR Systems®. This Interface Description Document (IDD) defines electrical interface requirements for the Quark 2.0 release. Changes or updates relative to the Quark 1.0 release are highlighted through the document in blue text.

Note: A number of expansion cards intended for specific applications are available for Quark. In most cases, these expansion cards modify or augment the standard core interfaces. This IDD only applies to the standalone core.

2 Applicable Documents

The following documents form a part of this specification to the extent specified herein.

2.1 FLIR Systems Documents

102-PS241-40	Quark Product Specification
102-PS242-43	Tau 2 / Quark Software Interface Description Document

2.2 External Documents

ANSI/TIA/EIA-232 (formerly RS232)	Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange
ANSI/TIA/EIA-644	Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits
EIA-170A	Composite Analog Video Signal – NTSC for Studio Applications
ITU Rec. BT.656	Interface for digital component video signals in 525-line and 625-line television systems operating at the 4:2:2 level of Recommendation ITU-R BT.601

3 Electrical Interface Requirements

This document defines requirements for the following Quark interfaces:

- Power
- Analog video data
- Digital video data
  - Parallel channel (single-ended)
  - Serial channel (LVDS)
- Discrete I/O (user-configurable)
- Frame-sync interface (optional)
- Communication interface
- Shutter interface
- ADC interface

3.1.1 Interface Connector

a. The electrical interface to the core is via a single high-density 60-pin connector: Samtec #ST4-30-1.50-L-D-P-TR. The connector is a board-to-board connector, and FLIR recommends using a rigid mount connector which screws into the board to provide proper connector strain relief. The recommended mating connector is Samtec #SS4-30-350-L-D-K-TR where XXX signifies a 3.50mm height for a mated stack height of 5mm. Connectors of different stack heights are available.

b. Generic pin definitions are shown in Table 1. See Figure 1 for a picture showing the pin numbering of the connector.

c. The pins defined as “XP1_” and “XP2_” in Table 1 are reconfigurable by the user (via the serial comm. interface).

i. Table 2 shows the definition of the XP bus as a function of the selected XP mode.

ii. Currently the XP2 bus is unused. It is anticipated that in future releases of the Quark, the XP2 bus will provide the option of a generic SPI bus, SDIO bus, and/or I2C bus.

Table 1: Primary I/O Connector Generic Pin Definition

Pin #	Signal Name	Pin #	Signal Name
1	LVDS_DATA2_N (see 3.1.4.3)	2	LVDS_CLK_N (see 3.1.4.3)
3	LVDS_DATA2_P (see 3.1.4.3)	4	LVDS_CLK_P (see 3.1.4.3)
5	LVDS_DATA1_N (see 3.1.4.3)	6	LVDS_FRAME_N (see 3.1.4.3)
7	LVDS_DATA1_P (see 3.1.4.3)	8	LVDS_FRAME_P (see 3.1.4.3)
9	DGND	10	DGND
11	SHUTTER0 (see 3.1.8)	12	VIDEO_HI (see 3.1.3)
13	SHUTTER1 (see 3.1.8)	14	VIDEO_LO (see 3.1.3)
15	RS232_RX (see 3.1.7)	16	RS232_TX (see 3.1.7)
17	DGND	18	DGND
19	ADC1 (see 3.1.9)	20	ADC0 (see 3.1.9)
21	PS_SHDN_N (see 3.1.2)	22	XP2_D10
23	XP2_D9	24	XP2_D8
25	XP2_D7	26	XP2_D6
27	XP2_D5	28	XP2_D4
29	XP2_D3	30	XP2_D2
31	XP2_D1	32	XP2_D0
33	XP2_CLK1	34	XP2_CLK0
35	DGND	36	DGND
37	XP1_D1	38	XP1_D0
39	XP1_D3	40	XP1_D2
41	XP1_D5	42	XP1_D4
43	XP1_D7	44	XP1_D6
45	XP1_D9	46	XP1_D8
47	XP1_D11	48	XP1_D10
49	XP1_D13	50	XP1_D12
51	XP1_D15	52	XP1_D14
53	XP1_D17	54	XP1_D16
55	XP1_CLK1	56	XP1_CLK2
57	DGND	58	DGND
59	PWR_IN (see 3.1.2)	60	PWR_IN (see 3.1.2)

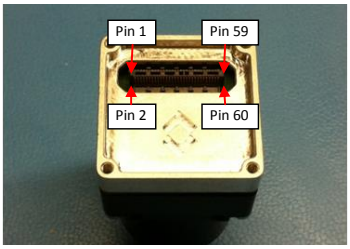


Figure 1: Primary I/O Connector Pinout, Samtec #ST4-30-1.50-L-D-P-TR

Table 2: XP1 Bus Reconfigurable Pins

XP1 Bus Signal	Pin #		XP1 Mode (Field-Selectable)			
		BT.656 (see 3.1.4.1)	CMOS 16-bit	CMOS 14-bit (see 3.1.4.2)	CMOS 8-bit (see 3.1.4.2)	Data Disabled
XP1_CLK1	55	BT656_CLK	CMOS_CLK	CMOS_CLK	CMOS_CLK	z
XP1_CLK2	56	z	EXT_SYNC	z	z	z
XP1_D0	38	BT656_D0	CMOS_D0	CMOS_D0	CMOS_D0	z
XP1_D1	37	BT656_D1	CMOS_D1	CMOS_D1	CMOS_D1	z
XP1_D2	40	BT656_D2	CMOS_D2	CMOS_D2	CMOS_D2	z
XP1_D3	39	BT656_D3	CMOS_D3	CMOS_D3	CMOS_D3	z
XP1_D4	42	BT656_D4	CMOS_D4	CMOS_D4	CMOS_D4	z
XP1_D5	41	BT656_D5	CMOS_D5	CMOS_D5	CMOS_D5	z
XP1_D6	44	BT656_D6	CMOS_D6	CMOS_D6	CMOS_D6	z
XP1_D7	43	BT656_D7	CMOS_D7	CMOS_D7	CMOS_D7	z
XP1_D8	46	DISCRETE5	CMOS_D8	CMOS_D8	DISCRETE5	DISCRETE5
XP1_D9	45	DISCRETE4	CMOS_D9	CMOS_D9	DISCRETE4	DISCRETE4
XP1_D10	48	DISCRETE3	CMOS_D10	CMOS_D10	DISCRETE3	DISCRETE3
XP1_D11	47	DISCRETE2	CMOS_D11	CMOS_D11	DISCRETE2	DISCRETE2
XP1_D12	50	z	CMOS_D12	CMOS_D12	z	z
XP1_D13	49	EXT_SYNC	CMOS_D14	EXT_SYNC	EXT_SYNC	EXT_SYNC
XP1_D14	52	DISCRETE1	CMOS_D13	CMOS_D13	DISCRETE1	DISCRETE1
XP1_D15	51	DISCRETE0	CMOS_D15	DISCRETE0	DISCRETE0	DISCRETE0
XP1_D16	54	DISCRETE_7	CMOS_FRAME_VALID	CMOS_FRAME_VALID	CMOS_FRAME_VALID	DISCRETE7
XP1_D17	53	DISCRETE_6	CMOS_LINE_VALID	CMOS_LINE_VALID	CMOS_LINE_VALID	DISCRETE_6

Note: Purple font = output signal. Blue font = Input or Output. z = high impedance

3.1.2 Power Interface

a. The Quark provides full functionality when voltage as specified in Table 3 is applied across PWR_IN and DGND.

Note 1: Quark does not provide protection against reverse-voltage or over-voltage.

Note 2: DGND serves as both power return and signal return.

b. A second option for powering down the Quark (instead of removing PWR_IN) is to short the PWR_SHDN_N pin to DGND. This pin should be disconnected for normal operation.

c. Certain user commanded operations such as saving settings to flash or updating firmware require power to be provided for the duration of the operation. The interruption of power during a flash operation may leave the camera in an unusable state.

Table 3: Quark Input Power Requirements

Parameter	Value	Notes
Input voltage	3.3V +/ 0.1V	*Voltage in excess of this value may cause permanent damage to the core.*
Average Power Dissipation	See below.	*Varies by configuration and varies over temperature*
Surge current at start-up	< 600 mA	*Duration < 8 msec*

Table 4: Quark 1.0 Power Dissipation

Quark Configuration	Power at 25C	Power at 80C
336	≤ 1.00W	≤ 1.15W
640	≤ 1.10W	≤ 1.25W

Table 5: Quark 2.0 Power Dissipation

Quark Configuration	Power at 25C	Power at 80C
336	≤ 1.00W	≤ 1.15W
640, 30Hz	≤ 1.15W	≤ 1.45W
640, 60Hz	≤ 1.35W	≤ 1.70W

Note1: The values above assume a single digital channel (BT.656, CMOS, or LVDS) is enabled and that the analog channel is disabled. The values are increased by approximately 65 mW by disabling all digital channels and instead enabling analog.

Note2: The power dissipation has slightly increased with the Quark 2.0 release due to the significant increase in the available feature set.

3.1.3 Analog Video Channel

a. The Quark provides analog video on the signals named VIDEO_H and VIDEO_L. Figure 2 shows required termination of the analog video channel. For transmission of the video channel, a coaxial cable with 75 ohm characteristic impedance is required.

b. The timing and voltage level of the analog video signal complies with either NTSC or PAL protocol. The choice between NTSC or PAL is user-selectable (via the serial comm. interface).

c. The channel may be disabled (via the serial comm. interface) for a savings of approximately 75 mW.

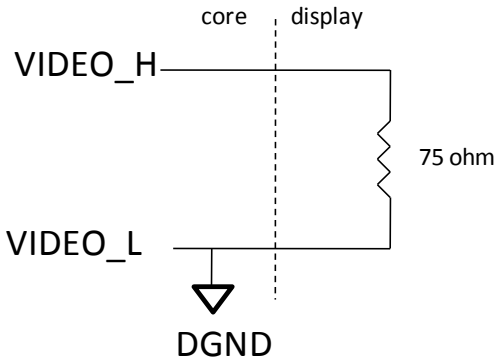


Figure 2: Required Termination of the Analog Channel

3.1.4 Digital Data Channels

a. The Quark provides the option of two simultaneous digital output channels, one parallel and one serial.

b. One or both channels can be disabled for a power savings of approximately 10 mW per channel.

c. The parallel channel can be field-configured to provide data via BT.656 protocol or a CMOS protocol, defined further in 3.1.4.1 and 3.1.4.2, respectively. Maximum recommended transmission length is approximately 1 m.

d. The serial port employs an LVDS protocol further defined in 3.1.4.3. Maximum recommended transmission length is approximately 3 m.

Note: Because the BT.656 and CMOS outputs are provided on a reconfigurable XP Bus available to multiple interface types / data rates, external signal filtering is required to minimize radiated emissions. For a specific XP-bus configuration and customer application, signal and power filtering should be tailored when targeting a given EMI specification. It is recommended that filtering be located immediately after the Quark mating connector. The filter type should address the extended harmonic frequencies of the XP Bus signaling and not cripple the signal shape and timing. The filter could be in the form of a series resistor or ferrite bead. The Quark chassis provides a flat metallic surface and four (4) mounting screw locations to fasten a mating PCB or Flex PCB. This surrounding chassis-attachment concept is the same as a cable shield.

3.1.4.1 BT.656 Protocol

The Quark provides the option of configuring the XP1 bus to provide digital output with timing/format in compliance with ITU Recommendation BT.656.

Note: This interface is fully compliant with the Recommendation except in terms of line driver characteristics, ECL-compatibility, and connector type.

1. The channel consists of a clock and 8 parallel bits of data, transmitted via single-ended 3.3V CMOS logic levels. See Table 2 for pin assignments.
2. The channel can only be configured for 8-bit (post-AGC) data. Symbol overlay and colorization are included in this output.
3. Clock frequency is 27 MHz. Refer to the ITU Recommendation for detailed timing / format requirements.
4. Frame rate is 29.97 Hz (NTSC) or 25.00 Hz (PAL). For the 336 "fast" configurations, each data field is duplicated once (i.e., 2 fields per frame) whenever the averager feature is enabled. (See the Quark Product Specification for more information on fast and slow configurations and the averager feature.) For the 640 fast configurations and for the 336 fast configurations with averager disabled, each BT.656 field contains unique data.
5. For "slow" configurations, each data field is duplicated multiple times to produce an *effective* frame rate $\leq$ 9Hz.

3.1.4.2 CMOS Protocol

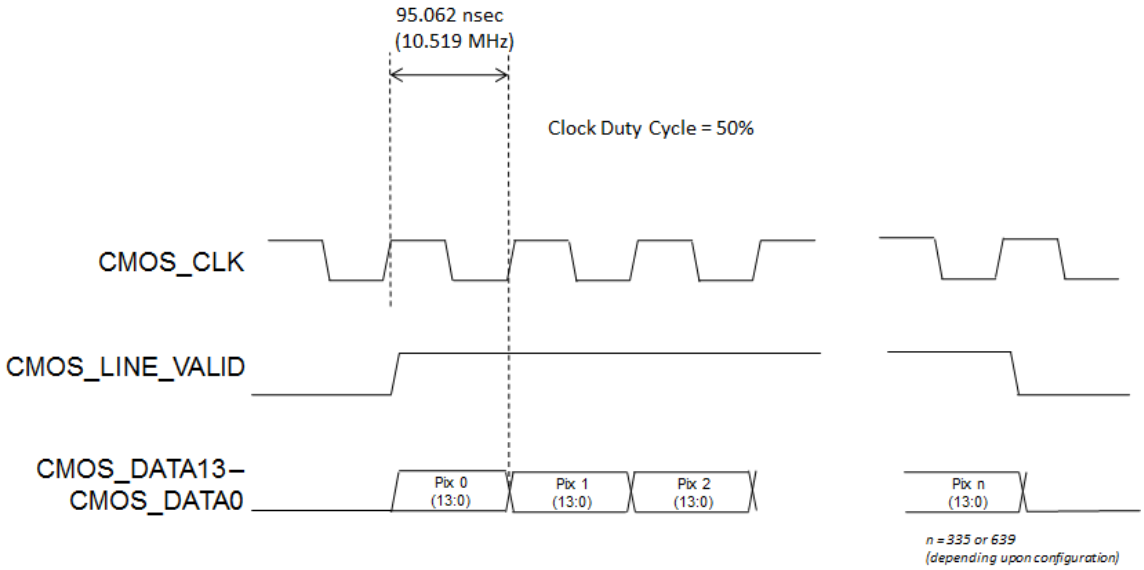
The Quark provides the option of configuring the XP1 bus to output a digital data protocol resembling that of a typical CMOS camera. Specifically:

1. The channel consists of a clock, up to 14 parallel bits of data, a line-valid signal, and a frame-valid signal. The channel utilizes 3.3V CMOS logic levels. Table 2 for pin assignments.
2. The choice between 14-bit (pre-AGC), 8-bit (post-AGC), 8-bit Bayer colorized, 16-bit YCbCr, and 8-bit double-clocked YCbCr data is field-selectable.
3. The field-selectable choice between 8-bit data with or without the continuous electronic zoom capability is also available. The "digital eZoom Mode" affects frame rate, resolution, and flat-field correction (refer to the Quark Product Specification for further details). In the 8-bit digital eZoom mode with colorization enabled (via the Bayer or YCbCr modes) the user also has the option to enable symbology in the 8-bit channel.
4. Line timing is depicted in Figure 3. The clock rate is 21.04MHz for the 640, 60Hz configuration. The clock rate is 10.519MHz for all other configurations (e.g. 640, 30Hz and 336). The clock for the 8-bit YCbCr mode is doubled such that the clock rate is as follows: 42.08MHz for the 640, 60Hz configuration and 21.04MHz for the 640, 30Hz and 336 configurations.
5. The Bayer and YCbCr colorization modes are both user configurable. The Bayer encoding order is user-selectable. The YCbCr order is configurable for the 8-bit double-clocked mode ('YCbYCr' or 'CbYCrY'), and the sub-sampling is configurable for both 16-bit and 8-bit double-clocked modes ('4:2:2 centered' or '4:2:2 cosited'). See the Quark Product Specification for further details. Figure 3b and Figure 3c shows the line timing for the 8-bit double clocked YCbCr mode and 16-bit YCbCr respectively ('YCbYCr' order, 4:2:2 cosited sub-sampling).
6. Frame timing is depicted in Figure 4. The frame rate depends upon configuration and settings as shown in Table 6.
7. No data is output on the CMOS channel during each flat-field correction (FFC) period. That is, CMOS_LINE_VALID, CMOS_FRAME_VALID, and CMOS_DATA[0-13] are all disabled throughout FFC. While the "digital eZoom Mode" is enabled, the 8-bit data output continues during FFC. That is, the last frame before FFC is replicated during each FFC period. This mode does not affect the 14-bit data output.

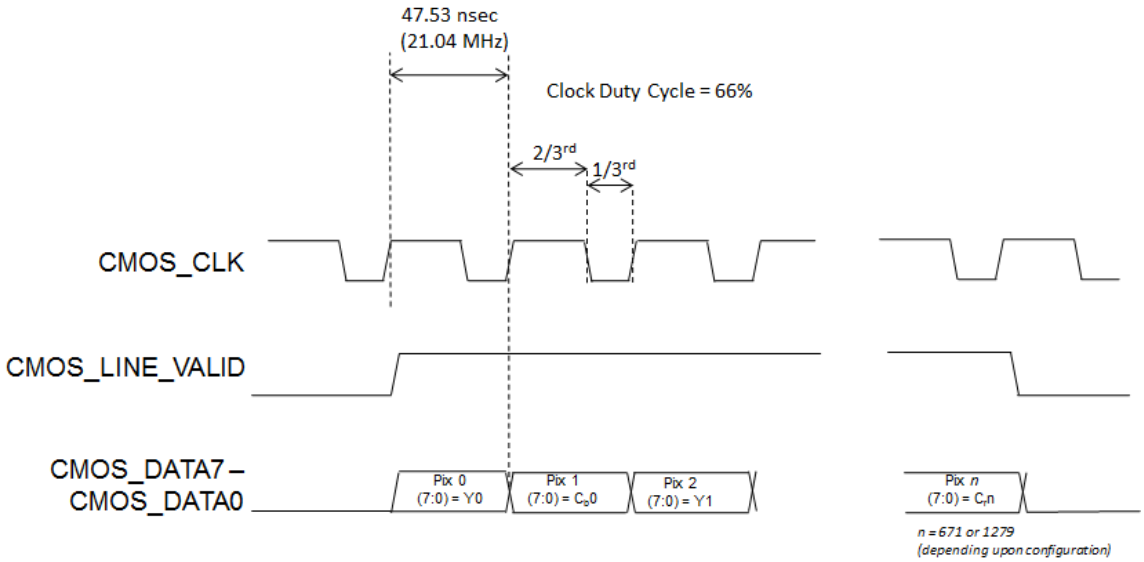
Table 6: Frame Rate vs. Configuration / Settings

Configuration, Video Speed	Configuration, Resolution	Video Setting	Averager Mode	Frame Rate (Hz)	Frame Rate (Hz) 8-bit Digital eZoom Enabled Mode
Fast	336	NTSC	Disabled	59.94 Hz	29.97 Hz
Fast	336	PAL	Disabled	50.00 Hz	25.00 Hz
Fast	336	NTSC	Enabled	29.97 Hz	29.97 Hz
Fast	336	PAL	Enabled	25.00 Hz	25.00 Hz
Fast	640, 30Hz	NTSC	not applicable	29.97 Hz	29.97 Hz
Fast	640, 30Hz	PAL	not applicable	25.00 Hz	25.00 Hz
Fast	640, 60Hz	NTSC	Disabled	59.94 Hz	59.94 Hz
Fast	640, 60Hz	PAL	Disabled	50.00 Hz	50.00 Hz
Fast	640, 60Hz	NTSC	Enabled	29.97 Hz	29.97 Hz
Fast	640, 60Hz	PAL	Enabled	25.00 Hz	25.00 Hz
Slow	336	NTSC	Disabled	7.49 Hz	29.97 Hz
Slow	336	PAL	Disabled	8.33 Hz	25.00 Hz
Slow	336	NTSC	Enabled	7.49 Hz	29.97 Hz
Slow	336	PAL	Enabled	8.33 Hz	25.00 Hz
Slow	640, 30Hz	NTSC	not applicable	7.49 Hz	29.97 Hz
Slow	640, 30Hz	PAL	not applicable	8.33 Hz	25.00 Hz

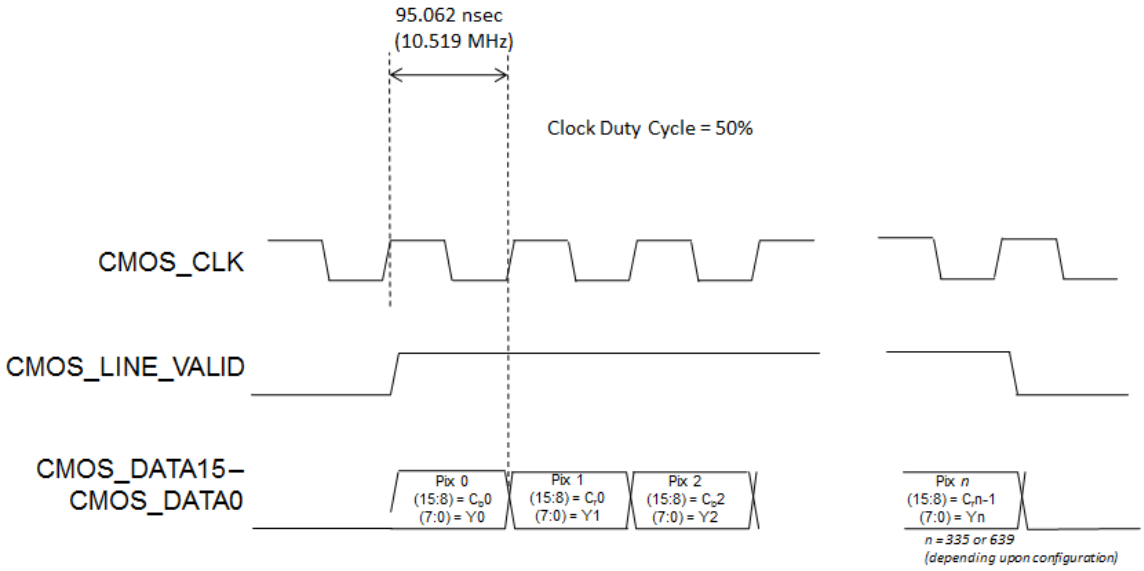
- *Note 1: The resolution value listed in the above table is that shown in the part number of the Quark. See the Quark Product Specification for further description. It refers to the number of pixel columns.*
- *Note 2: See the Quark Product Specification for a description of the averager feature.*
- *Note 3: The idle time at the end of each frame varies considerably depending upon frame rate and number of pixels per frame.*
- *Note 4: For Quark 2.0 and later releases, the optional "digital eZoom Mode" causes the frame rate to be either 29.97Hz or 25Hz, depending on video setting, with the exception of the 640, 60Hz configuration. For slow configurations, the frame rate is made up of replicated frames for a true data update rate of only 7.49Hz or 8.33Hz.*
- *Note 5: For Quark 2.0 and later releases, the optional "digital eZoom Mode" also affects the output resolution. The output resolution for the 8-bit CMOS and LVDS channels in this mode will be 640x512 regardless of the native array size.*



(a) 14-bit CMOS mode



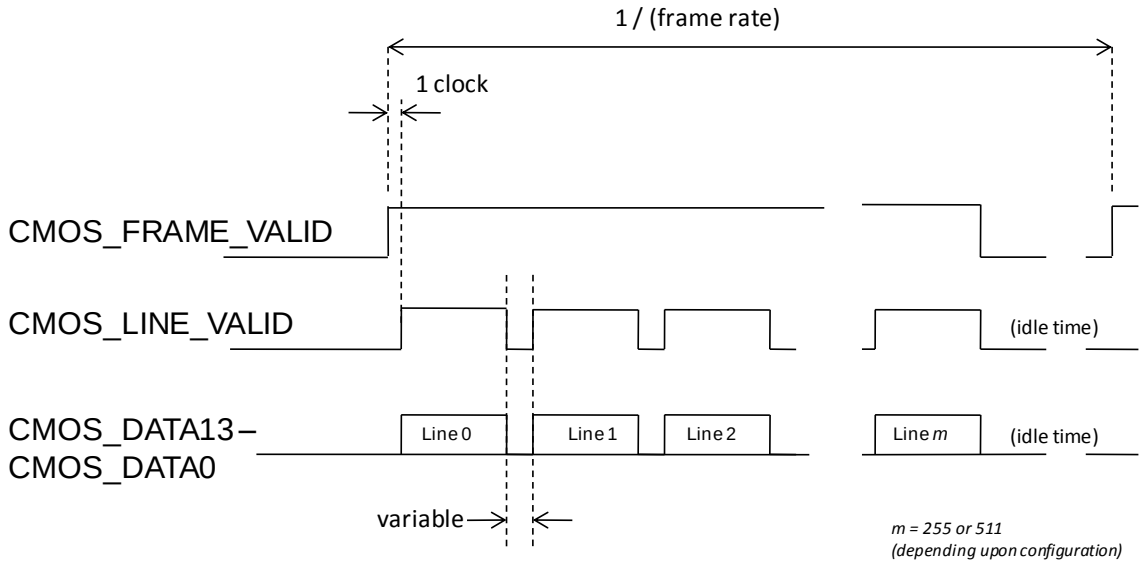
(b) 8-bit Double-Clocked YCbCr CMOS mode ('YCbYCr' 4:2:2 Cosited)



(c) 16-bit YCbCr CMOS mode (4:2:2 Cosited)

Note: Figures are not necessarily to scale

Figure 3: Line Timing, CMOS Protocol



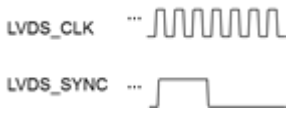
Note: Figure is not to scale.

Figure 4: Frame Timing, CMOS Protocol

3.1.4.3 LVDS Protocol

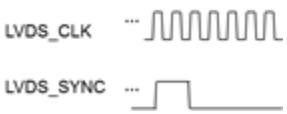
The Quark provides the option of a digital data protocol used on previous FLIR products including Photon and Tau. Specifically:

1. The channel consists of a clock pair, an encoded sync pair, and two data-line pairs. See Table 1 for pin assignments. All signals employ low-voltage differential signaling (LVDS).
2. The choice between 14-bit (pre-AGC), 8-bit (post-AGC), and 8-bit Bayer colorized data is field-selectable.
3. The field-selectable choice between 8-bit data with or without the continuous electronic zoom capability is also available. The "digital eZoom Mode" affects frame rate, resolution, and flat-field correction (refer to the Quark Product Specification for further details). In the 8-bit digital eZoom mode with colorization enabled (via the Bayer mode) the user also has the option to enable symbology in the 8-bit channel.
4. The clock rate is 147.27MHz for the 640, 60Hz configuration. The clock rate is 73.636MHz for all other configurations (e.g. 640, 30Hz and 336). One pixel datum is transmitted in each 7-clock period.
5. One sync datum is also transmitted in each 7-clock period. There are three possible 7-bit output values of the sync datum when the LVDS channel is active:
    a. Frame start: 1110000, as depicted in Figure 5a. The frame-sync datum is transmitted 4 pixel periods prior to the start of the first pixel of the first line.
    b. Line valid: 1100100, as depicted in Figure 5b. The line-valid datum is transmitted coincident with each valid pixel on the data lines.
    c. Data invalid: 1100000, as depicted in Figure 5c. The data-invalid datum is transmitted whenever there is no valid data on the data lines.
6. Line timing and sync encoding are shown in Figure 5d. Note that the idle portion of each line varies by configuration but is constant per line. That is, each line spans the same number of clock periods.
7. Phasing of the clock relative to the sync and data signals is shown in Figure 6.
8. The frame rate is identical to that of the CMOS channel as shown in Table 6.
9. No data output is output on the LVDS channel during each FFC period. That is, LVDS_SYNC and LVDS_DATA are both disabled throughout FFC. For Quark 2.0 and later releases, while the "digital eZoom Mode" is selected, the 8-bit data output continues during FFC. That is, the last frame before FFC is replicated during each FFC period. This mode does not affect the 14-bit data output.

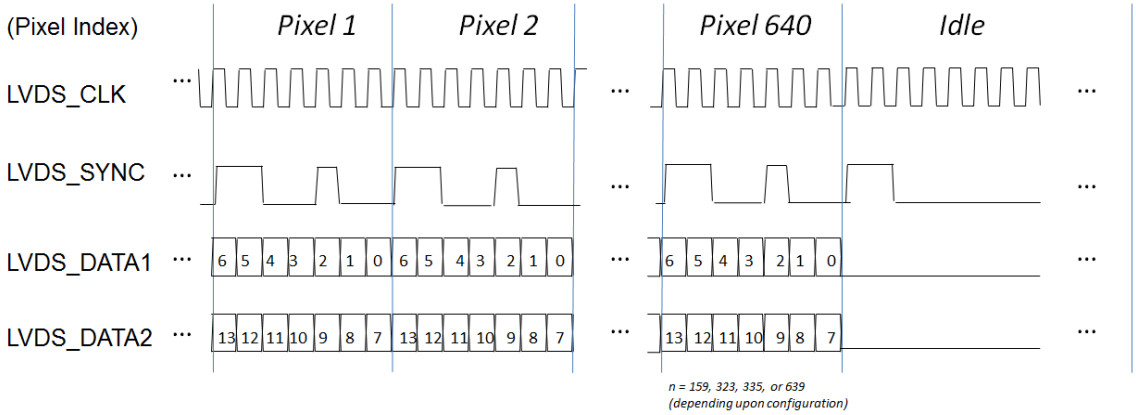


(a) LVDS_SYNC signaling frame start

(b) LVDS_SYNC signaling line valid



(c) LVDS_SYNC signaling data invalid



(d) LVDS Line Timing

Figure 5: Digital Data Timing, LVDS Protocol

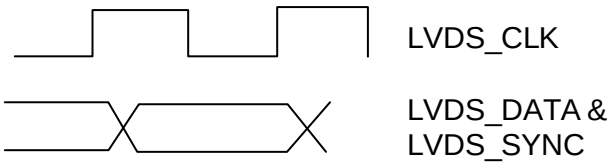


Figure 6: Digital Data Timing, LVDS Clock relative to Data and Sync

3.1.5 Configurable Discrete I/O Pins

Depending upon the XP bus mode (see Table 2), the Quark provides up to 8 signals referred to as discrete I/O pins (DISCRETE0 – DISCRETE7) that can each be field-configured to provide a specified functionality when shorted to DGND. For example, one of the pins might be configured to toggle between white hot and black hot polarity. The full list of functions that can be assigned to these pins is defined in the Quark Product Specification. There is no de-bounce circuitry on the signals. They are polled at 30Hz.

3.1.6 Frame Synchronization Interface

The Quark provides the option of transmitting or receiving a frame-synchronization pulse on EXT_SYNC. This feature provides the capability to synchronize frame start between two cores, one configured as master and the other configured as slave, or to synchronize the Quark with a different camera. Note that the synchronization state (master, slave, or disabled) must be preconfigured prior to power-up (i.e., the camera must be re-started after changing the mode and saving as a power-on default).

3.1.6.1 Master Mode

When configured as a master, the core transmits a pulse on the frame-synchronization interface at a rate of once per frame. The frame rate is dependent on the video standard (29.97/59.94Hz for NTSC or 25/50Hz for PAL) and for the Quark 2.0 release and later, is also dependent on the averager feature applicable for all configurations except the 640, 30Hz configuration. The frame rate is 59.94/50Hz with the averager disabled and 29.97/25.00Hz with the averager enabled for NTSC and PAL respectively. The pulse complies with the characteristics defined in Table 7.

Table 7: Sync Pulse Characteristics

Mode	Signal Direction	Voltage (relative to DGN)	Frequency Range	Pulse width (minimum)
Master	Output	3.3V	29.97/59.94Hz NTSC, 25.00/50Hz PAL	1 µsec
Slave NTSC, 30Hz (avg enabled)*	Input	3.3V	24.98Hz to 29.98Hz	100 nsec
Slave PAL, 25Hz (avg enabled)*	Input	3.3V	22.25Hz to 27.25Hz	100 nsec
Slave NTSC, 60Hz (avg disabled)*	Input	3.3V	54.94Hz to 59.94Hz	100 nsec
Slave PAL, 50Hz (avg disabled)*	Input	3.3V	47.25Hz to 52.25Hz	100 nsec
Disabled	n/a	3.3V	n/a	n/a

**Note: The 640, 30Hz configuration supports only 30Hz/25Hz modes.*

3.1.6.2 Slave Mode

When configured as a slave, the core synchronizes the FPA frame start to the rising edge of a pulse received on the frame-synchronization interface. The required frequency and pulse width are defined in Table 7. The frequency input is dependent on the configuration of the camera regarding video standard (NTSC/PAL) and averager (enabled/disabled) settings. If the camera is configured as NTSC with averager enabled (or simply NTSC for the 640, 30Hz configuration), any pulses sent at a rate greater than 30Hz will be ignored. (For example, if pulses are sent at 40 Hz (25 msec period), the pulse sent 25 msec after the first will be ignored. The next frame will be triggered on the next pulse for an effective frame rate of 20 Hz.) When in slave mode, the core will not output data until a valid pulse is received. Operating at a frequency different from those specified for each configuration in the table is not recommended due to degradation in image quality.

Note 1: Slave mode is not recommended for synchronizing analog video; this feature is intended for digital video synchronization. For a core configured as a slave, analog video output requires that the pulse timing be sent at a rate confirming to the selected video standard (either NTSC or PAL).

Note 2: The LVDS / CMOS frame sync signals are delayed relative to the External-Frame-Sync pulse. Consequently, digital frame acquisitions should use the appropriate sync signal and not rely on the External Frame Sync pulse for synchronization.

For slow configurations, the output frame rate is a fraction of the sync pulse rate. Because there is ambiguity as to which received pulse triggers the frame timing, FLIR does not recommended to use the external sync interface with a slow-configured Quark.

3.1.7 Communication Channel

The Quark provides an asynchronous serial interface consisting of the signals named RS232_RX (input to core), RS232_TX (output from core), and DGND. The interface complies with the RS232 standard except in voltage levels: Full RS-232 levels may be applied to the input, but 3.3V CMOS signal levels are output. The Quark automatically detects the polarity of incoming messages (standard logic or inverted logic) and replies at the same polarity. The Quark is capable of communication at various baud rates, as further described in the Quark Software IDD. The communication protocol of the RS232 channel is also defined in the Quark Software IDD.

3.1.8 Shutter Interface

The Quark provides two logic outputs, SHUTTER0 and SHUTTER1, intended to signal when to open / close an external shutter device. (These signals are logic signals only and are not intended to directly drive a shutter assembly.) The interface utilizes 3.3V CMOS logic levels. See the Quark Product Specification for further information regarding the intended use of these signals. If the Quark is not interfaced to an external shutter, these signals are otherwise unused. If SHUTTER0 and SHUTTER1 are interfaced to a shutter, it is possible to program the timing of the signals to match the drive characteristics of the selected shutter assembly.

3.1.9 ADC Interface

To be specified in a later release. The current release of Quark does not provide this interface.

This product is protected by patents, design patents, patents pending, or design patents pending.

If you have questions that are not covered in this manual, or need service, contact FLIR Commercial Systems Customer Support at 805.964.9797 for additional information prior to returning a camera.

This documentation and the requirements specified herein are subject to change without notice.

This equipment must be disposed of as electronic waste.
Contact your nearest FLIR Commercial Systems, Inc. representative for instructions on how to return the product to FLIR for proper disposal.

FCC Notice. This device is a subassembly designed for incorporation into other products in order to provide an infrared camera function. It is not an end-product fit for consumer use. When incorporated into a host device, the end-product will generate, use, and radiate radio frequency energy that may cause radio interference. As such, the end-product incorporating this subassembly must be tested and approved under the rules of the Federal Communications Commission (FCC) before the end-product may be offered for sale or lease, advertised, imported, sold, or leased in the United States. The FCC regulations are designed to provide reasonable protection against interference to radio communications. See 47 C.F.R. §§ 2.803 and 15.1 et seq.

Industry Canada Notice. This device is a subassembly designed for incorporation into other products in order to provide an infrared camera function. It is not an end-product fit for consumer use. When incorporated into a host device, the end-product will generate, use, and radiate radio frequency energy that may cause radio interference. As such, the end-product incorporating this subassembly must be tested for compliance with the Interference-Causing Equipment Standard, Digital Apparatus, ICES-003, of Industry Canada before the product incorporating this device may be: manufactured or offered for sale or lease, imported, distributed, sold, or leased in Canada.

Avis d'Industrie Canada. Cet appareil est un sous-ensemble conçu pour être intégré à un autre produit afin de fournir une fonction de caméra infrarouge. Ce n'est pas un produit final destiné aux consommateurs. Une fois intégré à un dispositif hôte, le produit final va générer, utiliser et émettre de l'énergie radiofréquence qui pourrait provoquer de l'interférence radio. En tant que tel, le produit final intégrant ce sous-ensemble doit être testé pour en vérifier la conformité avec la Norme sur le matériel brouilleur pour les appareils numériques (NMB-003) d'Industrie Canada avant que le produit intégrant ce dispositif puisse être fabriqué, mis en vente ou en location, importé, distribué, vendu ou loué au Canada.

EU Notice. This device is a subassembly or component intended only for product evaluation, development or incorporation into other products in order to provide an infrared camera function. It is not a finished end-product fit for general consumer use. Persons handling this device must have appropriate electronics training and observe good engineering practice standards. As such, this product does not fall within the scope of the European Union (EU) directives regarding electromagnetic compatibility (EMC). Any end-product intended for general consumer use that incorporates this device must be tested in accordance and comply with all applicable EU EMC and other relevant directives.